

14. The transistor of claim **1**, wherein the shield plate edge is configured to achieve a predetermined electrical characteristic of the shield plate.

15. A semiconductor device including, the customized shield plate FET comprising:

- a semiconductor layer including a surface layer extending from an upper surface of the semiconductor layer to a surface depth;
- a gate dielectric overlying the surface layer;
- a gate electrode including a first sidewall and a second sidewall defining lateral boundaries of a channel region of the surface layer;
- a shield interlevel dielectric (ILD) including a portion overlying at least a portion of an upper surface of the gate electrode, the first sidewall, and a drift region of the surface region, the drift region being adjacent the channel region;
- a customized shield plate comprising a conductive layer overlying at least a portion of the shield ILD, the shield plate defining a customized shield plate edge overlying the drift region, wherein a portion of the customized shield plate edge is non parallel to the second sidewall.

16. The semiconductor device of claim **15**, wherein the customized shield plate FET comprises a lateral diffused metal oxide semiconductor transistor.

17. The semiconductor device of claim **15**, wherein a second shield plate overlying at least a portion of the customized shield plate.

18.-20. (canceled)

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